**Amendments to the Specification:**

The Examiner has noted that the first page of the specification must include the following statement: "This application is a CIP (Continuation-in-Part) of Application serail Number 10/453,369, filed on June 3, 2003."

Applicant respectfully points out that the information required by the Office Action has been provided. Please see Page 1, paragraph [0002], of the Specification under the heading "Cross Reference to Related Applications."

Please replace paragraph [0002] with the following amended paragraph:

**[0002]** This application is Continuation-in-Part of US Patent Application Serial Number 10/453,369, filed June 3, 2003, and entitled "SAR ANALOG-TO-DIGITAL CONVERTER WITH TWO SINGLE ENDED INPUTS," Atty. Dkt. No. CYGL-26,248, and is related to pending application entitled "NOISE CANCELLATION IN A SINGLE ENDED SAR CONVERTER," Serial No. 10/735,163; Atty. Dkt. No. CYGL-26,543; and pending application entitled "SAR DATA CONVERTER WITH UNEQUAL CLOCK PULSES FOR MSBS TO ALLOW FOR SETTLING," Serial No. 10/734,890; Atty. Dkt. No. CYGL-26,545; and pending application entitled "HIGH SPEED COMPARATOR WITH BLOCKING SWITCHES FOR SAR CONVERTER," Serial No. 10/735,164; Atty. Dkt. No. CYGL-26,550; and pending application entitled "COMMON CENTROID LAYOUT FOR PARALLEL RESISTORS IN AN AMPLIFIER WITH MATCHED AC PERFORMANCE," Serial No. 10/735,387; Atty. Dkt. No. CYGL-26,552," and pending application entitled "OPEN LOOP COMMON MODE DRIVER FOR SWITCHED CAPACITOR INPUT TO SAR," Serial No. 10/734,854; Atty. Dkt. No. CYGL-26,544, all pending applications filed December 12, 2003.

Please replace paragraph **[0004]** with the following amended paragraph:

## SUMMARY OF THE INVENTION

**[0004]** The present invention disclosed and claimed herein, in one aspect thereof, comprises a ~~data converter~~ differential comparator having positive and negative inputs and positive and negative outputs. A current source is provided for driving current from a supply to a common node with a differential pair of transistors also provided. This differential pair of transistors has one side of the source/drain paths thereof tied together and to the common node. The other side of each of the transistors in the differential pair is interfaced to the positive and negative outputs, respectively, for applying drive thereto. A first resistor load is provided that is disposed between the positive input and a supply reference opposite in polarity to the supply. A second resistor is disposed between the negative output and the supply reference. The gate of one of the transistors in the pair associated with the positive output is connected to the negative input. The gate of the other of the transistors in the pair is connected to the positive input. The current through the current source defines a common mode bias with a bias circuit provided for controlling the voltage on a first and a second output at the first and second resistors to be at a common mode voltage that is controlled by an external bias voltage when the positive and negative inputs are at substantially the same voltage. ~~converter for converting analog data on a differential data input having a positive analog input terminal and a negative analog input terminal to digital data. The data converter includes a first single ended successive approximation register (SAR) analog-to-digital converter for converting the analog signal on the positive analog input terminal to a first digital signal and a second single ended successive approximation register (SAR) analog-to-digital converter for converting the analog signal on the negative analog input terminal to a second digital signal. A circuit for combining the first and second digital signals as a digital output signal for the data converter that represents the difference between the analog signals on the positive and negative analog input terminals.~~